REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Applicants appreciatively acknowledge the Examiner's confirmation of receipt of Applicants' claim for priority under 35 U.S.C. § 119 and certified copy of German Patent Application 102 29 802.5, filed July 3, 2002.

Claims 1-12 are now in the application and are subject to examination. Claims 1, 4 and 7 have been amended. Claim 12 has been added. No claims have been canceled.

In the section entitled "Claim Rejections - 35 USC § 102", which appears on pages 4-6 of the above-identified Office Action, claims 1-3, 5, 7, 8, 10 and 11 have been rejected as being fully anticipated by U.S. Patent No. 6,539,505 to Dähn under 35 U.S.C. § 102(e).

In the section entitled "Claim Rejections - 35 USC § 103" which appears on pages 6-8 of the Office Action, claims 4, 6 and 9 have been rejected as being obvious over Dähn in view of U.S. Patent No. 6,072,737 to Morgan et al. (hereinafter Morgan) under 35 U.S.C. § 103(a).

The rejections have been noted and the claims have been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is found in the Specification of the instant application.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, *inter alia*, a test circuit for testing a memory circuit, the test circuit comprising:

> a data input line for providing test data to be written to the memory circuit;
>
> a comparator unit connected to said data input line and to the memory circuit, said comparator unit comparing expected values received over said data input line with the test data read from the memory circuit, the test data previously having been written to the memory circuit over said data input line; and
>
> a data change circuit connected between said data input line and the memory circuit, said data change circuit being controllable depending on a result of a comparison performed in said comparator unit such that when an error occurs, further test data can be written to the memory circuit in a manner altered by said data change circuit;
>
> said data change circuit passing the test data in an unaltered form to said memory circuit if no error occurs and passing the test data in an inverted form to said memory circuit if an error occurs.

Independent method claim 7 contain similar language, in that it calls for, *inter alia*:

passing the test data to the memory area in an unaltered form if no error occurs, and passing the test data to the memory area in an inverted form if an error occurs.

In addition, claim 4 has been placed in independent form and a new independent claim 12 has been added, which includes the subject matter of original claims 7 and 4.

As already pointed out in the Response filed March 27, 2006, the changeover device according to Dähn does nothing more than copy the comparison result into each of the memory banks which are not being tested and therefore does not change any test data to be written into the memory bank to be tested.

Furthermore, the changeover device performs no function which depends on a result of the comparison performed in the comparator unit since the comparison results are copied into the memory banks which are not being tested.

With regard to claim 4, which is now in independent form (and claim 12 which contains the limitations of claim 4), the Examiner refers to the Morgan reference, in which a person skilled in the art is taught to include XOR gates.

First of all, the XOR gates disclosed in Morgan are not connected between the data input line and the memory circuit,

but are connected in the data output line and have no feedback line which is coupled back to an input of the memory circuit.

Furthermore, the XOR gates of Morgan serve as the comparator unit and compare the data signals read out with data signals provided by the test control circuit and supply an output result to an externally provided memory tester.

If the Examiner is of the opinion that the XOR gates of Morgan may render obvious the data change circuit in the sense of the present invention, Morgan would not have a comparator unit and consequently Morgan could not be understood by a person skilled in the art as a test circuit since it could not be operable without a comparison device. Therefore, it is assumed that the XOR gates as shown in Morgan cannot be interpreted as the data change circuit in the sense of the present invention which is provided in addition to a comparison unit.

It is believed to be clear from the arguments provided above that the XOR gates shown in Morgan cannot render obvious the subject matter of claim 4.

Therefore, claim 4 has been placed in independent form by

combining the subject matter of claims 1 and 4, that is including the feature that the data change circuit has a controllable exclusive-OR gate which, depending on the control signal generated by the comparator device, passes the test data in an unaltered form to the memory unit or inverts the test data with the aid of an exclusive-OR function resulting in the further test data being altered test data. New claim 12 contains similar subject matter.

Furthermore, it is also noted that the XOR gates are not controllable in such a way that their function can be activated or deactivated.

It is therefore clear that Dähn does not show a data change circuit in which test data is passed in an unaltered form to a memory circuit if no error occurs, and in which the test data is passed in an inverted form to the memory circuit if an error has occurred. Dähn also does not show the steps of amended claim 7.

It is also clear that Morgan does not teach a controllable exclusive-OR function which, depending on the comparison, passes the test data in an unaltered form to the memory area or inverts the test data with an aid of an exclusive-OR function resulting in the further test data being altered

test data.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 1, 4, 7 and 12. Claims 1, 4, 7 and 12 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claims 1 or 7.

In view of the foregoing, reconsideration and allowance of claims 1-12 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time is required, petition for extension is herewith made. Any extension fee associated therewith should be charged to Deposit Account Number 12-1099 of Lerner Greenberg Stemer LLP.

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Amdt. dated 9/12/06
Reply to Office action of 6/13/06

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to Deposit Account Number 12-1099 of Lerner Greenberg Stemer LLP.

Respectfully submitted,

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LAG/lq

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